What is claimed is:

1. A semiconductor package comprising:

a semiconductor chip having a major surface and first pads formed on the major surface;

a package substrate having (a) opposite first and second major surfaces, (b) a side surface extending between the first and second major surfaces, (c) a pad forming region adjacent to and along said side surface, (d) second pads formed on the pad forming region, (e) external electrodes formed on the first major surface of said package substrate, wherein said second major surface of said package substrate is fixed to the major surface of the semiconductor chip, and wherein the external electrodes are electrically connected to the second pads;

bonding wires electrically connecting the first pads to the second pads; and

a sealing material covering the bonding wires and first and second pads.

2. A semiconductor package as set forth claim 1, further including a protrusion extending from the side surface of said package substrate to define

a step configuration, and wherein the pad forming region is formed on the protrusion of the step configuration.

3. A semiconductor package as set forth claim 1, wherein the package substrate is a printed circuit board.

4. A semiconductor package as set forth claim 1, wherein said semiconductor chip includes circuit elements formed on the major surface of said semiconductor chip.

5. A semiconductor package comprising:

a first package substrate having a concave portion;

a semiconductor chip, fixed within the concave portion, having a major surface and first pads formed on the major surface;

a second package substrate having (a) opposite first and second major surfaces, (b) a side surface extending between the first and second major surfaces, (c) a first pad forming region adjacent to and along said side surface, (d) second pads formed on the first pad forming region, (e) external electrodes formed on the first major surface of said package substrate, wherein the second major surface of said second package substrate is fixed to the major surface of

said semiconductor chip, and wherein the first external electrodes ar electrically connected to the second pads;

a third package substrate stacked into said first package substrate, said third package substrate having (a) an opening defined by an inner surface thereof, (b) opposite first and second major surfaces, (c) third pads formed on a second pad forming region located adjacent to and along the inner surface, and (d) second external electrodes formed on the first major surface of said third package substrate, wherein the second external electrodes are electrically connected to the third pads;

bonding wires electrically connecting the first pads to the second pads and the third pads; and

a sealing material covering the bonding wires and first and second pads.

6. A semiconductor package as set forth claim 5, further including a protrusion extending from the side surface of said second package substrate to define a step configuration and wherein the first pad forming region is formed on the protrusion of the step configuration.

7. A semiconductor package as set forth claim 5, wherein the inner

surface of said third package substrate has a step configuration and wherein the second pad forming region is formed on a portion of the step configuration.

8. A semiconductor package as set forth claim 5, wherein the first pad forming region is formed on the first major surface of said second package substrate and wherein the second pad forming region is formed on the third major surface of said third package substrate.

9. A semiconductor package as set forth claim 5, wherein said second and third package substrates are printed circuit boards.

10. A semiconductor package as set forth claim 5, wherein said semiconductor chip includes circuit elements formed on the major surface of said semiconductor chip.

11. A semiconductor package as set forth claim 5, wherein the first pads comprise inside pads and outside pads which are aligned in respective rows along a periphery of said semiconductor chip.

12. A semiconductor package as set forth claim 11, wherein the inside

pads are electrically connected to the second pads and the outside pads are electrically connected to the third pads.

13. A semiconductor package comprising:

a semiconductor chip having a major surface and first pads formed on the major surface;

a package substrate including (a) opposite first and second major surfaces, (b) an opening extending between said first and second major surfaces and defined by opposed first and second side surfaces, (c) a pad forming region extending along and proximate said first side surface, (d) second pads formed on said pad forming region, and (e) external electrodes electrically connected to said second pads and formed on the second major surface of said package substrate, wherein the second major surface of said package substrate is fixed to the major surface of said semiconductor chip such that said first pads are aligned within the opening;

bonding wires electrically connecting the first pads to the second pads; and

a sealing material covering the bonding wires and first and second pads.

14. A semiconductor package as set forth claim 13, wherein the pad forming region is formed on the first major surface of said package substrate.

15. A semiconductor package as set forth claim 13, further including a protrusion extending from the first side surface of said package substrate to define a step configuration and wherein the pad forming region is formed on the protrusion of the step configuration.

16. A semiconductor package as set forth claim 13, wherein the first pads comprise first inside pads and first outside pads which are lined the first and second side surfaces of said package substrate respectively, wherein the second pads comprise second inside pads and second outside pads which are lined the first and second side surfaces of said package substrate respectively, and wherein the first inside pads are electrically connected to the second inside pads and the second inside pads are electrically connected to the second outside pads.

17. A semiconductor package as set forth claim 13, wherein the package substrate is a printed circuit board.

18. A semiconductor package as set forth claim 13, wherein said semiconductor chip includes circuit elements formed on the major surface of said semiconductor chip.